300 GHz CMOS Video Detection using Broadband and Active Planar Antennas

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***Abstract*—Using CMOS transistors for terahertz detection is currently a disruptive technology that offers the direct integration of a terahertz detector with video preamplifiers. The detectors are based on the resistive mixer concept and performance mainly depends on the following parameters: type of antenna, electrical parameters (gate to drain capacitor and channel length of the CMOS device) and foundry. Two different 300 GHz detectors are discussed: a single transistor detector with a broadband antenna and a differential pair driven by a resonant patch antenna.**

I. INTRODUCTION

Detectors based on III-V semiconductors, particularly the GaAs and InGaAs alloys, dominate the fields of heterodyne and video detection millimetre and terahertz waves. Improving the performance of these room temperature detectors is a challenge, but improvements continue to be made. Only in the last few years has the potential of a disruptive competing technology, based on silicon field effect transistors, been recognised. Continuous improvements in CMOS technology have enabled the necessary few hundred nanometre scale, and smaller, structures to be realised. A number of groups have begun research and their test results from this relatively immature detector field are impressive in terms of response, noise and frequency coverage. Prototypes of a range of terahertz devices such as frequency multipliers, Schottky diodes and novel FET detectors have all been realised [1].

To understand the disruptive impact of silicon technology, one needs to note that the basic wafer material for III-V devices is expensive, and device area are minimised to maximise yield. Completed detectors are soldered or epoxied to an antenna structure, and a separate pre-amplifier is then connected. Large area arrays are thus composed of devices interfacing with individually antennas, the latter being in planar or feedhorn form. In comparison, by using commercial CMOS technology, everything that is needed for a staring imaging array can be integrated on one silicon wafer. This includes the planar antennas, detector devices, pre-amplifier components and connections to signal processing circuitry. Once the non-recurring foundry investment has been made, the processing costs and raw materials are comparatively inexpensive, offering a revolutionary alternative approach to detectors, detectors arrays and terahertz cameras.

In this paper the development of designs for single pixel FET video detectors for 300 GHz radiation, based on CMOS technology, is presented. The theoretical analysis of FET square-law power detector for this millimetre wavelength is introduced and two antenna configurations are proposed as the collecting element for these detectors. The first one is based on bow-tie antennas [2] with no ground plane and single-NMOS transistor as detector, while the second one is based on differential active patch antennas [3] and differential NMOS transistor pair as detector. The goal of the work is to analyse the effects of different types of antennas (differential and single-ended), submitted to two different foundries, with different transistor channel lengths, to obtain best performance.

II. FET SQUARE-LAW POWER DETECTOR

FET square-law power detectors at THz frequencies have been recently demonstrated [4] and the first monolithically integrated CMOS terahertz focal-plane array has been designed and validated [5]. The working principle at millimetre wavelengths is based on the self-mixing resistive square-law NMOS-FET power detector circuit, as shown in Figure 1. It is similar to a FET resistive mixer [6] where a capacitor C_{gd} is included in order to facilitate self-mixing ($V(t)_{RF} = V(t)_{LO}$). A planar antenna is used to concentrate the THz radiation into the transistor, increasing the effective cross-section. The signal generated by the detector circuit is the current I_d, which is given by the equation:

$$I_d = \frac{W}{L}\mu C_{ox}\frac{V_{RF}^2}{4} \tag{1}$$

where W and L are the width and length of the device channel, C_{ox} is the gate oxide capacitance, μ is the electron mobility and V_{RF} is the amplitude of the RF signal. The current responsivity of the detector, γ, can then be defined as

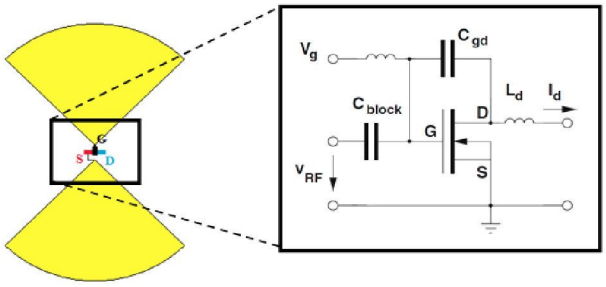
$$\gamma = \frac{I_d}{P_{RF}} \tag{2}$$

where P_{RF} is the power received by the antenna.

In a resistive mixer, the transistor has to be biased to operate in the Ohmic region. The channel of a FET, at low drain-to-source voltages, is a good approximation of a linear resistor. The resistance can be modulated by applying a LO

voltage to the gate. This voltage changes the depth of the depletion region under the gate and therefore the resistance of the channel. FET resistive mixers can achieve low conversion loss with low LO power [6].

Another advantage of resistive mixers is that RF input and IF output impedances are fortuitously usually around 50 Ω [6], so antennas can be designed to be matched to typical 50 Ω values and small losses are expected due to mismatch between antenna and active device. For accurate antenna design, RF input impedance and IF output impedance must be measured to minimize losses, as will be explained in the next section.



(a) (b)

Figure 1. Single NMOS detector: (a) planar bow-tie antenna with integrated FET and (b) circuit implementation of a self-mixing square-law NMOS-FET RF power detector circuit, from [5].

III. DETECTOR DESIGN

From the antenna point of view only two parameters can be optimized in order to maximize the responsivity of the detector: the radiation efficiency, ε_{rad}, and matching efficiency, M. The total efficiency can then be defined as the product of these two efficiencies and the polarization efficiency, ε_{pol}:

$$\varepsilon_{tot} = \varepsilon_{rad} \cdot M \cdot \varepsilon_{pol} \tag{3}$$

This efficiency expresses how far the system deviates from ideal detector performance. Maximizing ε_{tot} will enhance the performance of the detector and it is the key factor that we have used in the design of optimised planar antennas.

Two different topologies of detectors have been designed. The first, broadband, device consists of a bow tie antenna and a single resistive self-mixing NMOS transistor, as shown in Figure 1. The second, resonant, 300 GHz detector consists of differential patch antenna and a NMOS pair in a differential circuit configuration: Figure 2.

A. *Single NMOS detector*

With this configuration, low frequency dependence is expected because the bow-tie antenna has been designed to provide around 50Ω source impedance when placed over a silicon substrate. However, since no ground plane is included, it is expected that its radiation pattern will be adversely affected by substrate waves in the silicon wafer. The inclusion of a hyperhemispherical silicon lens is currently under study in order to avoid such undesired waves and to increase the directivity of the antenna. Different detecting NMOS FETs have been designed with channel lengths in the range 130 to 250 nm in order to study the effect on the frequency dependence and responsivity.

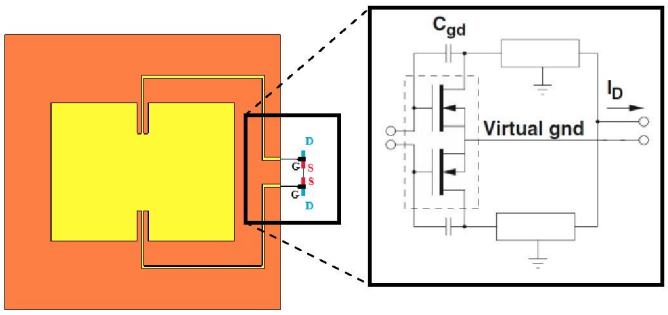
The bow tie antenna is a particular case of frequency independent antennas. Its input impedance is approximately given by [2]:

$$Z_{in} = \frac{60\pi}{\sqrt{\varepsilon_r}} \approx 55\Omega \quad (for\ silicon) \tag{4}$$

B. *Differential NMOS detector*

In this second configuration, a differential patch antenna and two NMOS FETs in a differential circuit topology have been designed. Patch antennas have many unique and attractive properties—low in profile, light in weight, compact and conformable in structure, and easy to fabricate and to be integrated with solid-state devices [2]. Differential patch antennas [3] have received great attention during last years for their use in radio systems.

This approach is expected to improve the overall behaviour because it can take advantage of both positive and negative signal cycles. In addition, differential patch antennas have a virtual ground on the symmetry axis. This removes the need for connecting the ground of the transistors with the antenna ground plane. As consequence, the parasitic effect caused by an interconnect is eliminated.



(a) (b)

Figure 2. Differential NMOS-pair detector: (a) differential patch antenna and two FETs and (b) circuit implementation of a self-mixing square-law differential NMOS-FET RF power detector circuit, from [5].

The differentially-driven microstrip antenna can be treated as a two-port network. Its input impedance is given by [3]:

$$Z_d = 2(z_{11} - z_{21}) = 2(z_{22} - z_{12}) \tag{5}$$

And the reflection coefficient:

$$\Gamma_{in} = s_{11} - s_{21} = s_{22} - s_{12} \tag{6}$$

when $s_{11}=s_{22}$ and $s_{21}=s_{12}$. Full theoretical analysis of this kind of antenna can be found in [3].

IV. DETECTOR MANUFACTURING

Two different foundries have been considered for the manufacturing of the prototypes. The main differences between them lies in the thickness of the metal and dielectric layers and the number of them, as well as material characteristics. An example of a typical CMOS manufacturing process can be seen on Figure 3.

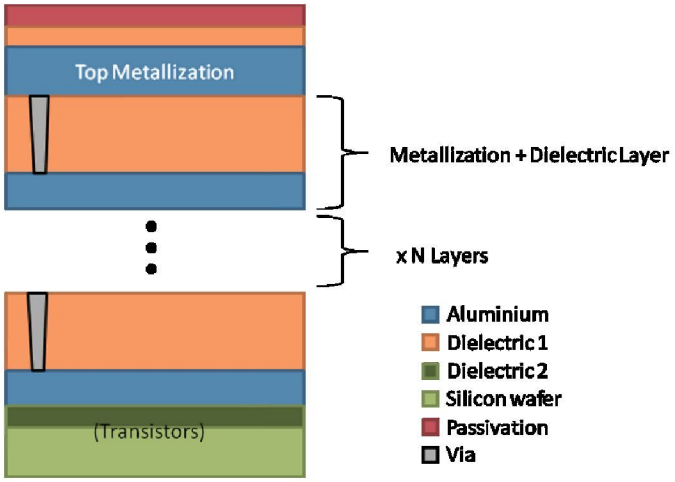


Figure 3. Example of a typical CMOS manufacturing process. The number of layers, dielectric constant, and thicknesses are foundry dependent.

For bow-tie designs, the lowest number of metallization + dielectric layers is used in order to reduce losses. Since this antenna has no ground plane, it is expected that radiation predominantly propagates into the high dielectric constant silicon substrate [8]. In order to reduce the effect of surface waves, as well as to increase the directivity of the antenna [8], a silicon hyperhemispherical lens will be included on the reverse of the silicon wafer. A typical lens of 10 mm diameter and 6.65mm thickness is used for simulation purposes: Figure 4. The corresponding numerical predictions can be seen in Figure 5. A directivity value of 24 dBi is obtained maintaining a reasonable value of radiation efficiency (77%).

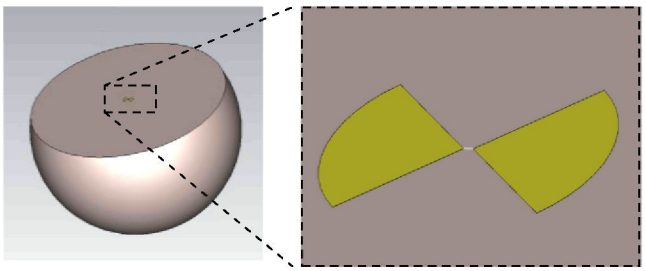
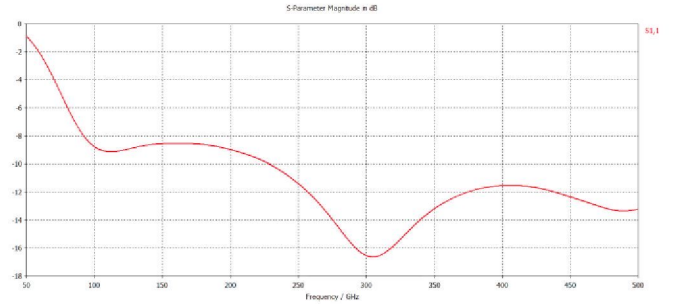
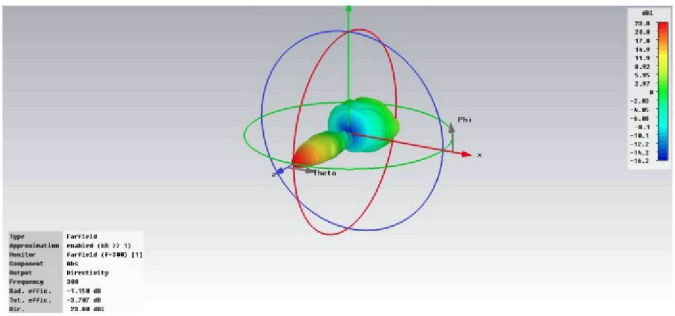


Figure 4. Schematic of the bow tie antenna with an underlying 10 mm diameter and 6.75 mm thickness hyperhemispherical silicon lens.



(a)



(b)

Figure 5. (a) Return losses of the bow tie antenna referred to 50 Ω and (b) radiation efficiency and 3D radiation pattern at 300 GHz.

On the other hand, in the design of the patch antennas, the ground plane is included in the metallization layer just above the dielectric 2 layer of Figure 3. In order to increase the radiation efficiency of the patch antenna, the maximum number of dielectric layers is included and aluminium layers in the substrate are removed. The metal patch is printed on the top metallization layer. As it can be seen from Figure 6, the thicker the dielectric layers, the higher the radiation efficiency is. CMOS technology processing does not readily deliver a layer thickness, h, greater than 20 μm. In our particular case, h is restricted to be below 15 μm so patch antenna radiation efficiencies lower than 60% expected. Since this antenna has a ground plane, no dielectric lens is necessary and a reasonably value of directivity is expected. Figure 7 shows the predicted results from a design optimised for one of the two foundries: this exhibits good performance in terms of both the return loss and the radiation efficiency (60%).

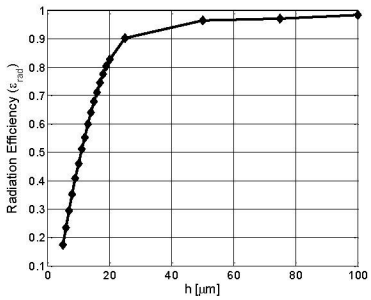
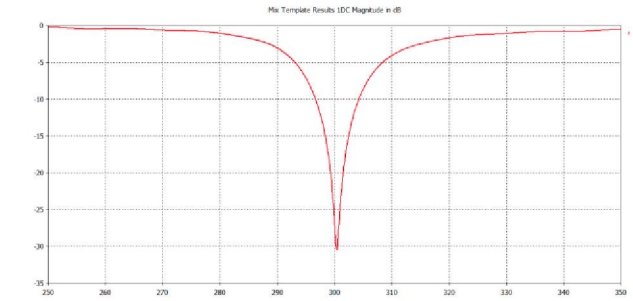
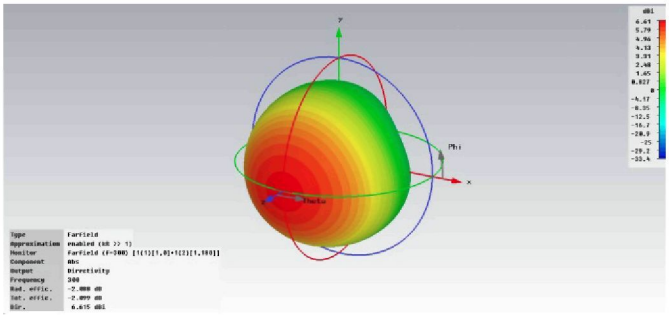


Figure 6. Simulated patch antenna radiation efficiency as a function of the total thickness of the dielectric layers for a frequency of 300 GHz.



(a)



(b)

Figure 7. (a) Return losses of the differential patch antenna referred to 50Ω. (b) Radiation efficiency and 3D radiation pattern at 300 GHz.

The mask top view of the manufactured detectors is shown in Figure 8. The smaller detectors are different patch antennas and bow-ties designed for 300 GHz detection. Three detectors for 100 GHz are also included (bigger patch, bow-tie and arc-ended bow-tie). These have also been optimised via the methods described above.

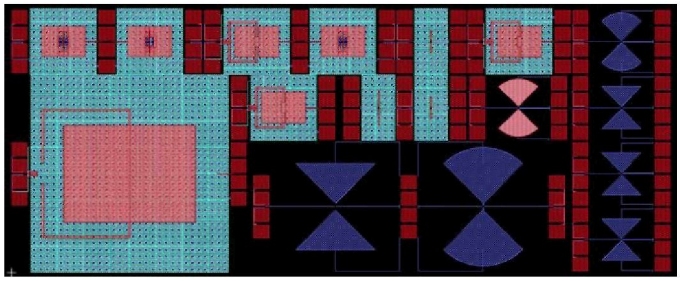


Figure 8. Mask top view of the manufactured detectors. Different colours represent the different metallization layers.

V. CONCLUSIONS

The development of designs of single pixel video detectors for THz radiation, based on CMOS technology, has been presented. The theoretical analysis of FET square-law power detector has been introduced and two antenna configurations with two FET circuits for 300 GHz detection have been presented.

From antenna point of view, total efficiency has been maximized to increase the responsivity of the detector. Radiation efficiency of both bow-tie and differential patch antenna has been maximized while mismatching efficiency will be very similar since both antennas have been designed to be matched to 50 Ω. This design methodology is reasonably good since RF input impedance of the active device is expected to be close to 50 Ω.

Two different foundries with different manufacturing capabilities have been selected to fabricate the prototypes, and processing is underway. The modelling is expected to be tested in the near future by measurements on fabricated devices in the laboratory.

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